

S/N 10/623,788**PATENT****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Leonard Forbes et al.	Examiner:	Pamela E. Perkins
Serial No.:	10/623,788	Group Art Unit:	2822
Filed:	July 21, 2003	Docket:	1303.109US1
Title:	STRAINED SEMICONDUCTOR BY FULL WAFER BONDING		

COMMUNICATION CONCERNING RELATED APPLICATIONS**MS AF**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/052,952 6,898,362	January 17, 2002	1303.034US1	THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD
10/382,246	March 5, 2003	1303.086US1	CELLULAR MATERIALS FORMED USING SURFACE TRANSFORMATION
10/379,749 7,198,974	March 5, 2003	1303.089US1	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
10/425,797 7,041,575	April 29, 2003	1303.093US1	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR
10/431,134 6,987,037	May 7, 2003	1303.094US1	STRAINED Si/SiGe STRUCTURES BY ION IMPLANTATION
10/425,484 7,220,656	April 29, 2003	1303.095US1	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/443,355 7,008,854	May 21, 2003	1303.098US1	SILICON OXYCARBIDE SUBSTRATES FOR BONDED SILICON ON INSULATOR
10/443,340	May 21, 2003	1303.099US1	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
10/431,137 7,115,480	May 7, 2003	1303.100US1	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
10/634,174 7,153,753	August 5, 2003	1303.102US1	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME

10/443,337	May 21, 2003	1303.103US1	GETTERING OF SILICON ON INSULATOR USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/623,794 6,929,984	July 21, 2003	1303.108US1	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
10/931,554 7,023,051	August 31, 2004	1303.093US2	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR
10/931,749 7,084,429	August 31, 2004	1303.095US2	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/931,344	August 31, 2004	1303.108US2	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
10/931,553	August 31, 2004	1303.099US2	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
10/931,580 7,045,874	August 31, 2004	1303.100US2	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
10/979,994	November 3, 2004	1303.102US2	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME
11/005,712 7,054,532	December 7, 2004	1303.034US2	THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD
11/210,927 7,202,530	August 24, 2005	1303.089US2	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
11/167,894	June 27, 2005	1303.108US3	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
11/210,373	August 24, 2005	1303.094US2	STRAINED Si/SiGe STRUCTURES BY ION IMPLANTATION
11/214,495	August 29, 2005	1303.098US2	SEMICONDUCTOR ON INSULATOR STRUCTURE
11/318,124	December 23, 2005	1303.095US3	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
11/497,632	August 2, 2006	1303.186US1	STRAINED SEMICONDUCTOR, DEVICES AND SYSTEMS AND METHODS OF FORMATION

11/353,406	February 14, 2006	1303.086US2	CELLULAR MATERIALS FORMED USING SURFACE TRANSFORMATION
11/432,578	May 11, 2006	1303.100US3	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
11/475,798	June 27, 2006	1303.109US2	STRAINED SEMICONDUCTOR BY FULL WAFER BONDING
11/493,128	July 26, 2006	1303.099US3	SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
11/460,391	July 27, 2006	1303.103US2	GETTERING OF SILICON ON INSULATOR USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
11/494,319	July 27, 2006	1303.102US3	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME
11/707,214	February 13, 2007	1303.089US3	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
09/855,532	May 16, 2001		METHOD OF FORMING MIRRORS BY SURFACE TRANSFORMATION OF EMPTY SPACES IN SOLID STATE MATERIALS
10/118,350	April 14, 2004		METHOD OF FORMING SPATIAL REGIONS OF A SECOND MATERIAL IN A FIRST MATERIAL
10/093,332	April 14, 2004		METHOD AND APPARATUS FOR PACKAGING SEMICONDUCTOR DEVICES

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 5-29-07 By Mar L R
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of May, 2007.

Lisa Resorlee
Name

Lisa Resorlee
Signature